Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1 – 23. (previously canceled)

24. (currently amended) A lighting system for graphics processing, comprising:

(a) at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;

(b) a multiplication logic unit coupled to the at least one input buffer;

(c) an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;

(d) a register unit coupled to the arithmetic logic unit; and

(e) a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit;

wherein the lighting logic unit is coupled to the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data.

25. (previously presented) The system as recited in claim 24, wherein the multiplication logic unit has a feedback loop coupled to an input thereof.

26. (canceled)

27. (previously presented) The system as recited in claim 24, wherein the arithmetic logic unit and the multiplication logic unit include multiplexers.

28. (previously presented) The system as recited in claim 24, wherein the multiplication logic unit includes three multipliers coupled in parallel.

29. (previously presented) The system as recited in claim 24, wherein the arithmetic logic unit includes three adders coupled in series and parallel.

30. (currently amended) A lighting system for graphics processing, comprising:

(a) at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;

(b) a multiplication logic unit coupled to the at least one input buffer;

(c) an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;

(d) a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit; and

(e) memory coupled to the multiplication logic unit and the arithmetic logic unit;

wherein the multiplication logic unit has a feedback loop coupled to an input of the multiplication logic unit.

31. (previously presented) The system as recited in claim 30, wherein the memory includes a plurality of constants for processing the vertex data.

32. (previously presented) The system as recited in claim 30, wherein the memory has a read terminal coupled to the multiplication logic unit.

33. (previously presented) The system as recited in claim 30, wherein the memory has a write terminal coupled to the arithmetic logic unit.

34. (currently amended) A lighting system for graphics processing, comprising:

(a) a multiplication logic unit;

(b) an arithmetic logic unit coupled to the multiplication logic unit;

(c) a register unit coupled to the arithmetic logic unit;

(d) a lighting logic unit coupled to the arithmetic logic unit and the multiplication logic unit; and

(e) memory coupled to the multiplication logic unit and the arithmetic logic unit;

wherein the multiplication logic unit has a feedback loop coupled to an input of the multiplication logic unit.

35. (canceled)

36-41. (previously canceled)